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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WOLDEGEORGIS, ERMIAS T	

ART UNIT	PAPER NUMBER
2893	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,828	SUZUKI ET AL.	
	Examiner	Art Unit	
	ERMIAS WOLDEGEORGIS	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,8,15-20 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,8,15-20 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/07/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Foreign Document*.

DETAILED ACTION

1. Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/31/2011 has been entered.

2. Response to Amendment

Claims 3-6, 9-14 and 21 have been cancelled; claims 1 and 16 have been amended; and claims 1-2, 7-8, 15-20 and 22-25 are currently pending.

3. Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

4. Information Disclosure Statement

The information disclosure statement (IDS) filed on 4/07/2011 has been acknowledged and a signed copy of the PTO-1449 is attached herein.

5. Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2, 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doczy et al. **(US 2004/0121541 A1, hereinafter "Doczy")** in view of Elers et al. **(US 2003/0082296 A1, hereinafter "Elers")** and Buchanan et al. **(USPN 5789312, hereinafter "Buchanan").**

In regards to claim 1, Doczy discloses (Fig. 8, annotated and attached below) a semiconductor device comprising: a semiconductor substrate **(10)**; a gate insulator **(30)** formed on the substrate **(10)**; and a gate electrode **(20)** having a metallic compound film **(WCN, Par[0024])** , the gate electrode **(20)** being formed on the insulator **(30).**

Doczy fails to explicitly teach the metallic film in the gate electrode is formed by CVD using a material containing a metal carbonyl, a C-containing material, and at least one of a Si-containing material and a N-containing material; the metallic compound film contains the metal **(W)** in the metal carbonyl, the C, and at least one of Si and the N**;** the work function of the metallic compound film can be controlled by changing the content of at least one of the Si and the N in the metallic compound.

Elers while disclosing a method for growing metal thin films (abstract) teaches a metallic compound film (**WN_xC_y, Par [0208]**) film formed by CVD (**ALD, Par [0208]**) using material containing a metal halide (**WF6, Par [0210]**), a C-containing material (**TEB, Par [0210]**), and at least one of a Si-containing material and a N-containing material (**NH_3, Par [0210]**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Doczy by Elers because as taught by Elers in par [0069], the ALD process would allow deposition of conformal metal thin films on an atomically thin level.

Doczy as modified by Elers fails to explicitly teach metal carbonyl.

Buchanan while disclosing a method of fabricating a mid-gap work-function tungsten gate (abstract) teaches metal carbonyl. (**$W(CO)_6$, col. 2 lines 59-62).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use tungsten carbonyl instead of tungsten halide because as taught by Buchanan in col. 2 lines 25-39, having tungsten carbonyl instead of tungsten halide (WF6) would make it possible for tungsten to be directly deposited onto ultra-thin gate dielectric materials. Also, the formation of tungsten gate using WF6 would make the silicon react away and form SiF4 even for thicker gate dielectric materials. Moreover, it has been determined that exposure of even quite thick oxide films to WF6 causes, without any exceptions, complete device failure owning to massive gate dielectric leakage currents.

Hence, Doczy as modified by Elers and Buchanan teaches the metallic compound film (**WCN**) contains the metal in the metal carbonyl (**W**) , the C (**C**), and the at least one of the Si and the N (**N**).

However, Doczy as modified by Elers abd Buchanan further fails to explicitly teach the work function of the metallic compound film can be controlled by changing the content of at least one of the Si and the N in the metallic compound.

It is well known in the art of manufacturing semiconductor devices to increase and decrease the concentration/content of the nitrogen for the purpose of controlling and/or optimizing the work function of metallic compound films -- the work function increases with the content of nitrogen in the metallic compound film.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to control the work function of the metallic compound film by changing the content of nitrogen because it is well known in the art of manufacturing semiconductor devices to increase and decrease the concentration/content of the nitrogen for the purpose of controlling and/or optimizing the work function of metallic compound films -- the work function increases with the content of nitrogen in the metallic compound film.

In regards to claim 2, Doczy discloses the metal is selected from the group consisting of W, Ni, Co, Ru, Mo, Re, Ta, and Ti **(Pars [0024]).**

In regards to claim 7, Doczy discloses the metallic compound film is doped with an n-type impurity or a p-type impurity **(see claim 19)**.

In regards to claim 15, Doczy discloses the metallic compound film **(WCN., Par [0024]**) used for a gate electrode of PMOS or NMOS of a MOS device **(PMOS, Par [0024]**)

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doczy in view of Elers and Buchanana as applied to claim 1 above, and further in view of Komatsu (**JP 10303412 , hereinafter "Komatsu")**.

In regards to claim 8, Doczy as modified above discloses all limitations of claim 1 but fails to explicitly teach the gate electrode further comprises a silicon film formed on the metallic compound film.

Komatsu discloses (Fig. 3) the gate electrode **(11)** further comprises a silicon film (**14**) formed on the metallic compound film **(13).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify Doczy by Komatsu because as taught by Komatsu in Par [0023], having a poly-silicon film on the metallic compound would help reduce the internal

stress generated by the metallic compound film while keeping the gate electrode thick enough to block ion implantation into the channel.

8. Claims 16-20, 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doczy in view of Elers, Buchanan and Matsuo et al. **(US 2003/0143825 A1, hereinafter "Matsuo")**.

In regards to claim 16, Doczy discloses (Fig. 8, annotated and attached below) a method for manufacturing a semiconductor device including a gate electrode **(20)** having a metallic compound film (**WCN, Par [0024]**).

Doczy fails to explicitly teach the method comprising:
preparing a material containing a metal carbonyl, a C-containing material and at least one of a Si- containing material and a N-containing material; and
forming, by CVD using the prepared materials, the metallic compound film so that the film contains the metal in the metal carbonyl, the C, and at least one of Si and N; wherein by controlling film deposition conditions, the content of the at least one of the Si and the N in the metallic compound film is adjusted such that the work function of the metallic compound film is in the mid-gap of Si.

Elers preparing a material containing a metal halide (**WF6, Par [0208]**) , a C-containing material (**TEB, Par [0208]**) and at least one of a Si- containing material and a N-containing material (**NH3, Par [0210]**); and

forming, by CVD (**ALCVD, Par [0210]**) using the prepared materials, the metallic compound (WN_xC_y, **Par [0208]**) film so that the film contains the metal (**W**) in the metal halide (**Par [0008] and Par [0208]**) , the C (**Par [0011] and Par [0210]**), and at least one of Si and N (**par [0011] and Par [0210]**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Doczy by Elers because as taught by Elers in par [0069], the ALD process would allow deposition of conformal metal thin films on an atomically thin level.

Doczy as modified by Elers fails to explicitly teach metal carbonyl.

Buchanan while disclosing a method of fabricating a mid-gap work-function tungsten gate (abstract) teaches metal carbonyl. **($W(CO)_6$, col. 2 lines 59-62).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use tungsten carbonyl instead of tungsten halide because as taught by Buchanan in col. 2 lines 25-39, having tungsten carbonyl instead of tungsten halide (WF6) would make it possible for tungsten to be directly deposited onto ultra-thin gate dielectric materials. Also, the formation of tungsten gate using WF6 would make the silicon react away and form

SiF4 even for thicker gate dielectric materials. Moreover, it has been determined that exposure of even quite thick oxide films to WF6 causes, without any exceptions, complete device failure owning to massive gate dielectric leakage currents.

However, Doczy modified by Elers and Buchanan further fails to teach controlling film deposition conditions, the content of the at least one of the Si and the N in the metallic compound film is adjusted such that the work function of the metallic compound film is in the mid-gap of Si.

Matsuo while disclosing a semiconductor device (abstract) teaches **(Fig. 2)** by controlling film deposition conditions, the content of the at least one of the Si and the N in the metallic compound film is adjusted such that the work function of the metallic compound film is in the mid-gap of Si **(see also Par [0041]).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify Doczy by the method and/or concept of Matsuo because as taught by Matsuo in Par [0043], it would be possible to make the threshold voltage of each of the n-type MISFET and P-type MISFET appropriate by optimizing the work function of the gate electrode included in each of the n-type MISFET and p-type MISFET.

In regards to claim 17, Doczy as modified by Elers, Buchana and Matsuo discloses the metal **(W, col. 4 line 6, Buchanan)** constituting the metal carbonyl **($W(CO)_6$, col. 4 line8, Buchanan**) is

selected from the group consisting of W, Ni, Co, Ru, Mo, Re, Ta, and Ti **(col. 4 lines 5-12, Buchanan).**

In regards to claim18, Doczy as modified by Elers, Buchana and Matsuo discloses the metal carbonyl is $W(CO)_6$ (**col. 4 lines 5-12, Buchanan)** .

In regards to claim 19, Doczy as modified by Elers, Buchanan and Matsuo discloses all limitations of claim 16 but fails to explicitly teach the Si-containing material is selected from the group consisting of silane, disilane, and dichlorosilane.

It is well known in the art to use silane, disilane or dichlorosilane as a source material for the purpose of introducing a silicon into the metallic compound during the formation of gate electrode.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate silane, disilane or dichlorosilane because it is well known in the art to use silane, disilane or dichlorosilane as a source material for the purpose of introducing a silicon into the metallic compound during the formation of gate electrode.

In regards to claim 20, Doczy as modified by Elers, Buchanan and Matsuo discloses the N-containing material is selected from the group consisting of ammonia and monomethyl hydrazine **(Par [0210], Elers)**.

In regards to claim 22, Doczy discloses (fig. 8, annotated and attached below) the metallic compound film is doped with an n-type impurity or a p-type impurity **(see claim 19).**

In regards to claim 25, Doczy discloses (fug. 8, annotated and attached below) the metallic compound film (**WCN, par [0024]**) is used for a gate electrode of pMOS or nMOS of a MOS device (**P-type, Par [0024]**).

9. Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doczy in view of Elers, Buchanan and Matsuo as applied to claim 16 above, and further in view of Komatsu.

In regards to claim 23, Doczy as modified by Elers, Buchanan and Matsuo discloses all limitations of claim 16 above but fails to explicitly teach forming a silicon film on the metallic compound film.

Komatsu discloses forming a silicon film **(14)** on the metallic compound film **(13).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a silicon film on the metallic compound film because as taught by Komatsu in the abstract and Pars [0014]-[0016], this would help alleviate the superfluous tensile stress to gate oxide by thinning the metallic compound film while the entire

gate electrode being thick enough by forming polysilicon on the metallic compound film. As a result of this, the reliability of the whole integrated circuit would be improved.

In regards to claim 24, Doczy as modified by Elers, Buchanan and Matsuo discloses all limitations of claim 21 above but fails to explicitly teach the C- containing material is selected from the group consisting of ethylene, allyl alcohol, formic acid, and tetrahydrofuran.

However, it is known in the art of manufacturing semiconductor devices ethylene is used as carbon-containing source gas for the purpose of incorporating C into a metal compound film.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use ethylene as a carbon-containing source gas for the incorporation of C into metal compound film because it is known in the art of manufacturing semiconductor devices ethylene is used as carbon-containing source gas for the purpose of incorporating C into a metal compound film.

10. Response to Arguments

Applicant's arguments with respect to claims 1 and 16 have been considered but are moot in view of the new ground(s) of rejection.

11. Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERMIAS WOLDEGEORGIS whose telephone number is (571)270-5350. The examiner can normally be reached on Monday through Friday 8:30 AM to 6:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERMIAS WOLDEGEORGIS/
Examiner, Art Unit 2893